

Appl. No. 10/604,440
Amdt. dated July 06, 2006
Reply to Office action of March 06, 2006

Amendments to the Claims:

1. (currently amended) A method for ~~Peripheral Component Interconnect (PCI) Express~~
Packet Triggered Power Management (PM) (PTPM) using a Peripheral Component
5 Interconnect (PCI) PCI traditional level triggered PM mechanism in a computer
system, the computer system including a PCI level triggered Power Management
Event (PME) controller and a PCI PTPM Express Root Complex, the method
comprising:
converting a plurality of PM_PME packets generated by the PTPM ~~PCI Express~~
10 Root Complex into a Pseudo-PME signal, a first PM_PME packet of the
plurality of PM_PME packets asserting the Pseudo-PME signal so that a
voltage of Pseudo-PME signal changes from a first level to a second level;
providing a Pseudo-PME line electrically connected to a PME input of the PCIPME
controller and the PCI PTPM Express Root Complex for transmitting the
15 Pseudo-PME signal to the PCI PME controller, the PME input receiving
PME signals generated by other PCI-compliant level triggered devices
through a PCI Bus of the computer system; and
de-asserting the Pseudo-PME signal so that the voltage of the Pseudo-PME signal
changes from the second level to the first level, the de-assertion of the
20 Pseudo-PME signal following the assertion of the Pseudo-PME signal by a
predetermined time interval;
wherein the first level and the second level of the voltage of the Pseudo-PME signal
are PCI-compliant with the level triggered PME controller.
- 25 2. (original) The method of claim 1 wherein the PCI PME controller is a chipset of the
computer system.
3. (original) The method of claim 1 further comprising providing a sequential circuit to

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convert the PM_PME packets into the Pseudo-PME signal.

4. (original) The method of claim 3 wherein the sequential circuit is a latch or a flip-flop.
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5. (original) The method of claim 1 further comprising providing a timer to control a time interval between asserting and de-asserting the Pseudo-PME signal.
6. (original) The method of claim 1 further comprising converting a pulse of a PM_PME packet of the plurality of PM_PME packets into a lower frequency pulse to control a time interval between asserting and de-asserting the Pseudo-PME signal.
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7. (original) The method of claim 6 further comprising providing a synchronizer to convert the pulse of the PM_PME packet of the plurality of PM_PME packets into the lower frequency pulse.
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8. (original) The method of claim 6 wherein the lower frequency pulse is an active-low pulse and works as the Pseudo-PME signal in the computer system.
- 20
9. (original) The method of claim 1 wherein the PCI PME controller includes an event register which can be set by the PCI PME controller when the Pseudo-PME signal is asserted but cannot be cleared when the Pseudo-PME signal is de-asserted, the method further comprises clearing the event register with a program of the computer system.
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10. (original) The method of claim 9 wherein the program is a device driver of the computer system.

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11. (currently amended) A computer system comprising:
- a Packet Triggered Power Management (PTPM) PCI Express-Root Complex for generating a plurality of PM_PME packets;
 - 5 a sequential circuit electrically connected to the PCI PTPM ~~Express~~-Root Complex for converting the plurality of PM_PME packets into a Pseudo-PME signal;
 - a PCI PME controller comprising an event register, the event register for reporting a power management event to the computer system;
 - a Pseudo-PME line electrically connecting an output of the sequential circuit to a
 - 10 PME input of the PCI PME controller, the event register being cleared when the Pseudo-PME signal changes from a first level to a second level; and
 - a memory comprising computer code executed by the computer system when voltage of the Pseudo-PME signal changes from the second level to the first level, the computer code capable of clearing the event register;
 - 15 wherein the first level and the second level of the voltage of the Pseudo-PME signal are PCI-compliant with the level triggered PME controller.
12. (original) The computer system of claim 11 further comprising a timer connected to the sequential circuit to control when voltage of the Pseudo-PME signal is changed
- 20 from the second level to the first level.